REMARKS

The present Amendment is in response to the Examiner's Office Action mailed December 15, 2006. Claims 1, 6, 9, 11, and 17 are amended. Claims 1-26 are now pending in view of the above amendments.

Reconsideration of the application is respectfully requested in view of the above amendments to the claims and the following remarks. For the Examiner's convenience and reference, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

Please note that the following remarks are not intended to be an exhaustive enumeration of the distinctions between any cited references and the claimed invention. Rather, the distinctions identified and discussed below are presented solely by way of example to illustrate some of the differences between the claimed invention and the cited references. In addition, Applicants request that the Examiner carefully review any references discussed below to ensure that Applicants' understanding and discussion of the references, if any, is consistent with the Examiner's understanding.

I. PRIOR ART REJECTIONS UNDER 35 U.S.C. §102(e)

The Examiner rejected claim 14 under 35 U.S.C. §102(e) as being anticipated by United States Patent Application Publication No. 2004/0179138 to Wang et al. ("*Wang*"). Because *Wang* does not teach or suggest each and every element of claim 14, Applicants respectfully traverse this rejection in view of the following remarks.

Claim 14 recites, among other things, "receiving an asserted synchronization signal from a phase locked loop ... [and] determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency...." In contrast, the Examiner has not established that *Wang* teaches the aforementioned limitations.

The Examiner asserted that *Wang* discloses the aforementioned limitations in the abstract and at paragraph [0053]. *See* Office Action, p. 2 (citing *Wang* at abstract, lines 5-6, 9-11, 12-15). Applicants respectfully disagree. The abstract describes a "frequency phase-locked loop detector (17) for supplying an output signal indicating whether an intermediate frequency demodulator is in an unlocked mode ... or in a locked mode" and "a video detector (18) for

detecting a video property in the incoming signal." As a preliminary matter, it is unclear what portion of the cited passages corresponds to the claimed "asserted synchronization signal" and clarification is respectfully requested.

Moreover, the Examiner has not established that *Wang* describes "determining whether [a] synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed. For this claim limitation, the Examiner referred to paragraph [0053], which states that "[i]f the PLL detection circuit 17 is locked, the first phase detector 6 is switched on." Checking the status of a PLL detection circuit, however, does not constitute "determining whether [a] synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed.

Since *Wang* does not teach or suggest each and every element of claim 14, Applicants respectfully request that the rejection under 35 U.S.C. § 102(e) be withdrawn.

II. PRIOR ART REJECTIONS UNDER 35 U.S.C. § 103

Applicants respectfully note at the outset that in order to establish a prima facie case of obviousness, it is the burden of the Examiner to demonstrate that the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See MPEP* § 2143. Moreover, the Examiner must "identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed." *See* U.S. Patent and Trademark Office Memorandum entitled *Supreme Court decision on KSR Int'l. Co. v. Teleflex, Inc.*, May 3, 2007. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *See MPEP* § 2143.01.V.

A. Rejections Based on Wang

The Examiner rejected claims 1-3, 9, 10, and 15 under 35 U.S.C. § 103 as being unpatentable over *Wang* in view of "The 555 Timer Tutorial" by Tony van Roon ("*van Roon*"); rejected claims 4 and 5 as being unpatentable over *Wang* and *van Roon* as applied to claim 3, and further in view of "Transistors" at www.electronics-tutorials.com ("*Transistors Tutorial*"); rejected claims 16 and 17 as being unpatentable over *Wang* as applied to claim 14, and further in view of U.S. Patent No. 5,886,748 to Lee ("*Lee*"); rejected claims 6, 7, 11, and 12 as being

unpatentable over *Wang* and *van Roon* as applied to claim 2, and further in view of *Lee*; rejected claim 8 as being unpatentable over *Wang*, *van Roon*, and *Lee*, as applied to claim 7, and further in view of "Phase-Locked Loop Protocol Scheme for a Synchronization Field," IBM Technical Disclosure Bulletin, May 1990 ("*IBM TDB*"); rejected claim 13 as being unpatentable over *Wang*, *van Roon*, and *Lee*, as applied to claim 12, and further in view of *IBM TDB*; and rejected claim 18 as being unpatentable over *Wang* as applied to claim 14, and further in view of *IBM TDB*.

Applicants traverse the Examiner's rejections for obviousness on the grounds that the references—either individually or in combination—fail to teach or suggest each and every element of the rejected claims.

1. Claims 1-8

Independent claim 1 recites, among other things, "[a] phase locked loop [that] keeps [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal; and a timing circuit that measures a period of time that the synchronization signal is asserted and produces a lock signal if the synchronization signal is asserted for at least a specified period of time."

The Examiner asserted that *Wang* discloses a phase locked loop that "keeps [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal ([0053]); [and] produces a lock signal if the synchronization signal is asserted for a least a specified period of time ([0051-[0053])...." *See* Office Action, p. 3. Applicants respectfully disagree. As a preliminary matter, it is unclear what portion of the cited passages corresponds to the claimed "synchronization signal" and clarification is respectfully requested.

Moreover, contrary to the Examiner's assertion, *Wang* does not describe producing a lock signal if another signal is asserted for at least the pause time, Tp. Instead, *Wang* describes pausing a channel search during the time Tp to allow a coincidence detection circuit to reach a final value. *See* paragraphs [0043] and [0055].

Therefore, *Wang* does not teach or suggest each and every element of claim 1. Furthermore, *van Roon*, *Transistors Tutorial*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of *Wang*. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for

obviousness and respectfully request that the rejection of claim 1, and corresponding dependent claims 2-8, be withdrawn.

2. Claims 9-13

Claim 9 recites, among other things, "a controller chip having a phase locked loop that ... is adapted to operate in a locked mode that asserts the synchronization signal so long as the phase locked loop is locked onto a data signal; and a translation circuit that converts the synchronization signal from the controller chip to a lock signal...." In contrast, the Examiner has not established that *Wang* discloses the aforementioned limitations. For example, the Examiner has not pointed to any description in *Wang* that corresponds to the claimed translation circuit. Applicants respectfully submit that this is because *Wang* discloses no such translation circuit. Furthermore, *van Roon*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of *Wang*. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for obviousness and respectfully request that the rejection of claim 9, and corresponding dependent claims 10-13, be withdrawn.

3. Claims 15-18

Applicants respectfully submit that insofar as the rejections of claims 15-18 rely on the unsupported assertions regarding the disclosure of *Wang* advanced by the Examiner in connection with the rejection of claim 14, such rejection lacks an adequate foundation, for at least the reasons outlined at section I above. Furthermore, *van Roon*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of *Wang*. Accordingly, the rejections of claims 15-18 should be withdrawn.

B. Rejections Based on Lee

The Examiner rejected claims 19 and 20 under 35 U.S.C. § 103 as being unpatentable over *Lee* in view of *van Roon*; rejected claim 21 as being unpatentable over *Lee* and *van Roon*, as applied to claim 20, and further in view of *Transistors Tutorial*; and rejected claims 22-26 as being unpatentable over *Lee* and *van Roon*, as applied to claim 19, and further in view of *IBM TDB*.

Applicants traverse the Examiner's rejections for obviousness on the grounds that a person of ordinary skill in the art would have no reason to combine the prior art elements in the

manner claimed because the proposed combination would render *Lee* unsatisfactory for its intended purpose.

Claim 19 requires, among other things, "a comparator circuit that compares the output signal [from a timing circuit] with a reference signal." The Examiner proposed combining a comparator circuit in *Lee* with a timing circuit in *van Roon*. The symbol timing and field sync restorer 114 in *Lee*, which was identified as the claimed comparator circuit (*see* Office Action, p. 10), compares a field reference signal with a field sync (*see Lee*, col. 2, lines 51-55). However, the field sync is constituted of 832 symbols (*see Lee*, col. 3, lines 10 and 11), whereas the timing circuit of *van Roon* outputs only one bit of data (*see van Roon*, Figure 3, p. 2). Thus, in the proposed combination, restorer 114 of *Lee* would compare a field reference signal with the one bit output from the *van Roon* timing circuit instead of the 832 symbol field sync. The comparison would therefore not be feasible or would at best yield meaningless results and the device would be unsatisfactory for its intended purpose of equalizing using a reference signal. *See Lee*, Title.

Furthermore, *Transistors Tutorial* and *IBM TDB*, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of the proposed combination of *Lee* and *van Roon*. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for obviousness and respectfully request that the rejection of claim 19, and corresponding dependent claims 20-26, be withdrawn.

III. REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

The Examiner rejected claims 6, 11, and 17 under 35 U.S.C. § 112, Second Paragraph for indefiniteness. The rejection has been obviated by the amendments made herein to each of claims 6, 11, and 17. Accordingly, withdrawal of the § 112 rejection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe the claims as amended are in allowable form. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, or which may be overcome by an Examiner's Amendment, the Examiner is requested to contact the undersigned attorney.

Dated this 10th day of May, 2007.

Respectfully submitted,

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